RAPID THERMAL SOLID PHASE EPITAXY ANNEALING FOR ULTRA-SHALLOW JUNCTION FORMATION

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Two of the key challenges according to the 2001 International Technology Roadmap for semiconductors for the source/drain extension junction at the 65-70 nm node and beyond are production of junctions between 10 and 19 nm with sheet resistance values between 760 to 830 ohm/sq. for low parasitic source/drain series resistance [1]. Ultra-shallow $^{49}BF_2^+$ and $^{11}B^+$ implants (4.5 keV and 500 eV respectively, $1.0 \cdot 10^{15}$ cm^{-2}) were implanted at room temperature into $^{73}Ge^+$ (30 keV, $1.0 \cdot 10^{15}$ cm^{-2}) pre-amorphized <100> Si. In contrast to fast spike anneals [2, 3] a simple alternative approach for the formation of ultra-shallow junctions with boron was chosen, consisting of a low-temperature (600-800°C, 5-90 s) solid-phase epitaxial growth process in a standard rapid thermal annealing system with tightly controlled gaseous ambient (NH_3, Ar, O_2). The advantage of this technique is that boron changes over to the electrically-active substitutional site during the regrowth process while dopant diffusion within the lattice is suppressed/minimized by the low temperature process.

INTRODUCTION

Doping technology in conjunction with annealing technology is expected to provide solutions for highly activated, shallower, and more abrupt dopant profiles especially for advanced-logic device technology beyond the 90 nm node [1]. Implantation of boron or BF_2 in combination with preamorphization and solid-phase epitaxial growth (SPEG) techniques currently appear to be promising for achieving junction depth and sheet resistance values low enough to meet the performance specifications. The SPEG technique is well known and understood for at least three decades including its advantage of leaving less residual disorder in regrown amorphous layers on <100>-oriented substrate compared to other orientations [4]. Crowder reported that the epitaxial growth already occurs at temperatures as low as 550°C and that the implanted dopants are activated during the defect-free regrowth of the amorphous layer [5, 6]. Therefore the dopant activation can be completely separated from diffusion and the resulting impurity profile abruptness nearly equals that of the as-implanted distribution. The disadvantage of SPEG is the residual damage. The remaining end-of-range damage below the recrystallized amorphous layer after SPEG may influence the electrical characteristic of the junction especially if this disorder is within the depletion region. Despite this

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disadvantage there are several examples where furnace SPEG has been integrated within advanced device processes including disposable spacers to suppress short channel effects without using a complex halo technique as well as for other novel device fabrication processes [7, 8, 9, 10]. In this contribution the state-of-the-art beamline ion implantation and lamp-based annealing technology are combined to demonstrate their synergy for shallow solid-phase epitaxial grown junctions with acceptable sheet resistance values, satisfying the R_s vs. X_J requirement for advanced devices.

EXPERIMENTAL PROCEDURES

For the experiments, 200 mm, n-type 10 – 20 Ωcm, prime (100) Si wafers were used. The samples used in this survey were implanted to a dose of $1.0 \cdot 10^{15}$ cm^{-2} with either $^{11}B^+$ (0.5 keV) or $^{49}BF_2^+$ (2.2 keV, 4.5 keV) into a $^{73}Ge^+$ preamorphized layer (30 keV $1.0 \cdot 10^{15}$ cm^{-2} , the upper edge of the end-of-range damage is at 45 nm). These implants were performed on a Varian VIISion-80 ULE high-current implanter at tilt and twist angles of 0° with electrostatic deceleration in front of the target. A key issue for these ultra-shallow implants of 100 to 200 Å depth is the variability of the native oxide. To avoid any influence prior to the implantation process a 30 s wet-chemical etch was performed in a HF (49 %):H_2O (1:40) solution. After implantation the wafers were cleaved into 2x2 cm^2 samples which were annealed in a Mattson rapid thermal processing (RTP) system on a recessed wafer. The samples were processed at various temperatures ranging from 600°C to 800°C, using annealing times in the range of 5 s to 90 s in Ar, NH_3, and various partial pressures of O_2 in Ar. These anneals illustrate the effects of differences in thermal budget, but also show the impact of the ambient on the solid-phase epitaxial regrowth. The sheet resistance was probed in a rectangular pattern on a KLA-Tencor RS100 using an H-type probe and 4 mm edge exclusion. The extrinsic dopant atom distributions were analyzed using secondary ion mass spectroscopy (SIMS) at Evans East Inc. (Physical Electronics 6600 Quadrupole SIMS, 1.0 keV O_2 beam at 60°). The near-surface concentration accuracy was optimized by using the O_2-leak technique. The chemical junction depth throughout this publication is defined as the depth where the total B concentration falls below a level of $1 \cdot 10^{18}$ cm^{-3} in the SIMS profile. For the measurement repeatability of SIMS, Magee et al. report that the relative standard deviation for the dose and the apparent junction depth, X_J, measurements are 5 % and 3.5 %, respectively [11].

RESULTS AND DISCUSSION

Thermal budget

Figure 1 shows for comparison the boron SIMS profiles after 600°C and 650°C SPEG processes for 10 s and 60 s. Whereas for the 650°C samples the SIMS profiles overlap, in case of the 10 s anneal at 600°C the regrowth process appears to be incomplete in the near-surface region. Just below the kink in the annealed profiles at a depth of 60 Å the profile for the 10 s is further from the surface than in the 60 s case,

whereas behind the kink the profiles overlap. The sheet resistance value of 405 Ω/□ indicates that the p^+n-junction is not fully formed at 10 s and the regrowth is not completed. For the BF_2 samples a similar effect appears for this thermal budget. This view is supported by data from Olson who measured the regrowth rate at 600°C for silicon implanted with boron or fluorine at to be around 59.8 Å/s and 0.94 Å/s, respectively [12]. Significant SPEG rate enhancement by the Fermi-level effect of boron doping or rate reductions from fluorine implants relative to the intrinsic level occur when the impurity concentration exceeds ~10^{20} cm^{-3} [13].

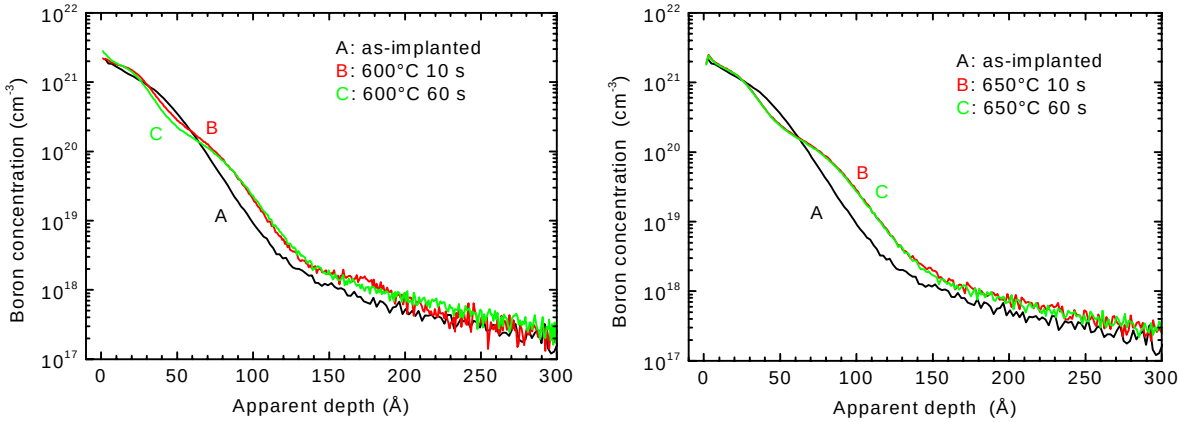

Figure 1: SIMS profiles of 500 eV boron, implanted to a dose of 1·10^{15} cm^{-2}, and after 600°C or 650°C for 10 s or 60 s annealing in pure argon gaseous ambient. **Left:** B: 405.55 Ω/□, C: 785.7 Ω/□; **Right:** B: 784.62 Ω/□, C: 797.64 Ω/□

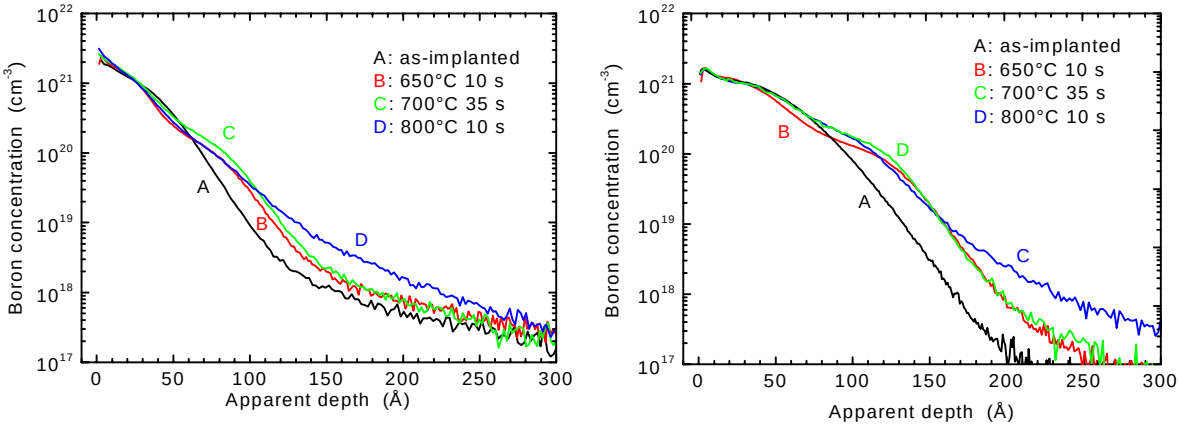

Figure 2: As-implanted and annealed boron SIMS profiles after 650°C and 800°C for 10 s, and 700°C 35 s annealing in pure argon gaseous ambient **Left**: $^{11}B^+$, 500 eV, 1.0·10^{15} cm^{-2}; B: 784.62 Ω/□, C: 765.56 Ω/□, D: 882.74 Ω/□ **Right:** $^{49}BF_2^+$, 4.5 keV, 1.0·10^{15} cm^{-2}; B: 812.39 Ω/□, C: 759.10 Ω/□, D: 780.74 Ω/□

At elevated temperatures, the regrowth rate is so high that the redistribution of dopants during solid-phase epitaxy, especially on <100>-oriented silicon, is usually negligible. Figure 2 shows a comparison of various annealing conditions on SIMS profiles for boron and $^{49}BF_2^+$ implanted samples. Significant broadening in the tail region (for boron < 4·10^{19} cm^{-3}, for $^{49}BF_2^+$ < 8·10^{18} cm^{-3}) of the profile only occurs for the 800°C 10 s process a. The reason for this strongly enhanced diffusion is certainly an

oversaturation of self-interstitials emanating from the end-of-range disorder. For the other temperatures and times the profiles are nearly identical, as also seen in Fig. 1. Although the boron is implanted into amorphous Si and the as-implanted junction is 100 Å shallower compared to comparable implantations into crystalline silicon, a profile tail is visible for $^{11}B^+$ implants which arises from incomplete decelerated boron. Whereas $^{49}BF_2^+$ profiles are much steeper down to boron concentrations much below $1{\cdot}10^{18}$ cm^{-3}. The lateral as well as vertical abruptness determined between boron concentration of $1{\cdot}10^{20}$ cm^{-3} and $2{\cdot}10^{18}$ cm^{-3}of the dopant profiles for temperatures below 700 °C were 3.5 nm/decade independent of the implant condition. At 800°C the respective values are 4.7 nm/decade for $^{49}BF_2^+$, and 5.3 nm/decade for $^{11}B^+$. The abruptness for the as-implanted distributions of $^{11}B^+$, $^{49}BF_2^+$ is 3.0 nm/decade.

Gaseous ambient

The influences of the ambient as well as of increasing annealing times on the resulting sheet resistance values are shown in Fig. 3. For the inert argon ambient at 650°C for 5 s the lowest sheet resistance value of 745 Ω/□ is reached. This corresponds to a solid solubility value of $1.9{\cdot}10^{20}$ cm^{-3} and is therefore close to the maximum limit of ~$3.5{\cdot}10^{20}$ cm^{-3} for a silicon preamorphized layer [14]. Above this level electrically inactive boron forms even for a low temperature solid-phase epitaxial process. The undissolved boron in the regrown layer favours/enhances the precipitation of the active fraction during the successive thermal processing of the sample [14]. In Fig. 3 it is obvious that the sheet resistance increases with prolonged annealing, especially at 800°C. For lower temperatures down to 650°C the changes are less pronounced. For all data points in the figure as well as for oxygen-ambient conditions the retained dose is found to be higher than 95% suggesting that outdiffusion is not the cause of the increase.

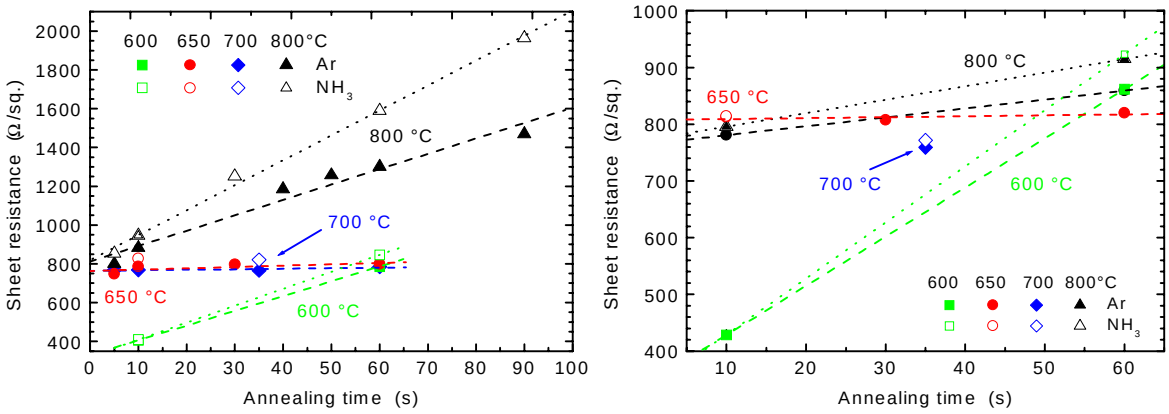

Figure 3: Summary of sheet resistance versus annealing time data for two gaseous annealing ambients (Ar: solid symbol, NH_3: hollow symbol). **Left:** $^{11}B^+$ 500 eV, $1.0{\cdot}10^{15}$ cm^{-2}, **Right:** $^{49}BF_2^+$ 4.5 keV, $1.0{\cdot}10^{15}$ cm^{-2}. The broken lines are linear regressions to the data. Deactivation rates: $^{11}B^+$, 800°C: Ar 7.93 (Ω/□)/s, NH3 12.87 (Ω/□)/s; $^{49}BF_2^+$ 800°C: Ar 1.57 (Ω/□)/s, NH3 2.38 (Ω/□)/s

For all the anneals in ammonia, the sheet resistance values were higher than those for the anneals in an argon ambient. This is especially evident for annealing at 800°C.

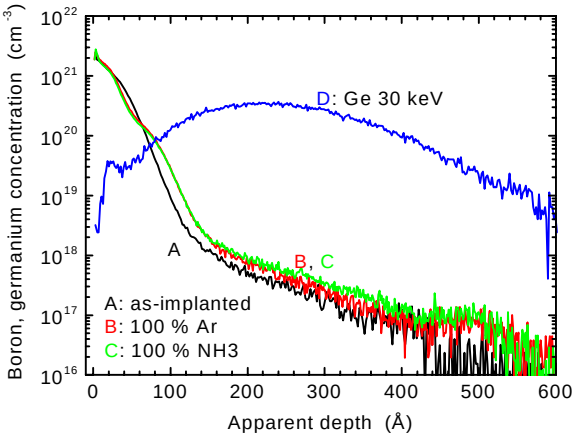

Figure 4: SIMS profiles of the as-implanted and subsequent SPEG boron annealed distributions in a 30 keV germanium pre-amorphised Si layer. ($^{11}B^+$, 500 eV, $1.0 \cdot 10^{15}$ cm^{-2}) to demonstrate the dependence of the SPER on the gaseous ambient for constant thermal budget (650°C 10 s). The sheet resistance values are as follows. B: 784.62 Ω/□ (100 % Ar), C: 826.45 Ω/□ (100 % NH_3).

This indicates that vacancy injection enhances the deactivation of boron with time. In an oxygen ambient, the sheet resistance also increases for temperatures up to 700°C but at elevated temperatures (> 950°C) a reduction is observed [15]. But the overall ambient influence on sheet resistance is much more pronounced in case of boron-only implantation while it is less dramatic with $^{49}BF_2^+$ (see Fig. 4). The fluorine seems to have a positive effect on the deactivation of boron. Independent of the implanted boron species neither an inert ambient like Ar nor reactive ambients like NH_3 (vacancy injection) or O_2 (silicon self-interstitial injection) have any significant influence on the boron SIMS profile. This is demonstrated in Fig. 4 for argon and NH_3 incase of $^{11}B^+$ implanted samples. Fig. 4 also shows the segregation/trapping of boron to/at the end-of-range damage region (450 Å - 550 Å) which is comparable for BF_2^+ [16].

Analysis of the experimental trends in the R_s vs. X_J figure

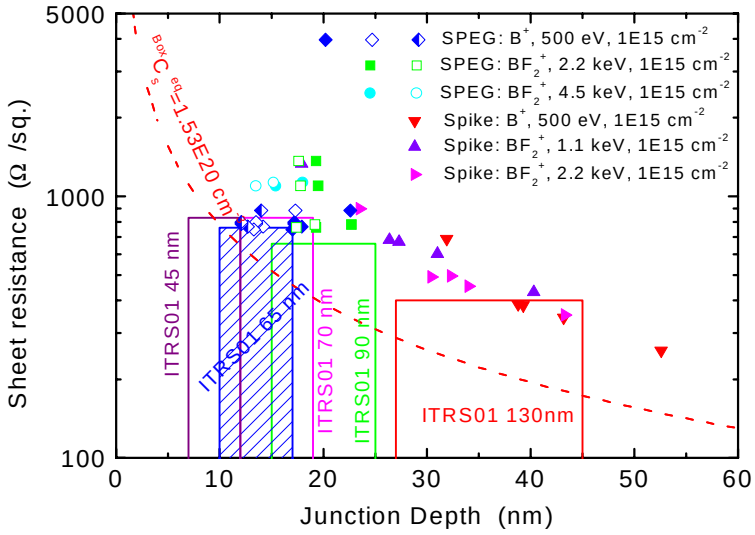

Figure 5: The Rs vs. Xj figure for p-channel source drain extensions compared to the ITRS 2001 requirements [1]. (Dashed curve: ideal box shape profile with a surface concentration of $1.53 \cdot 10^{20}$ cm^{-3} at 1050°C) The figure includes spike annealed data [2, 17] as well as SPEG data from this survey. Additionally, the hollow/half solid symbols denote the junctions formed by SPEG when X_j is measured at $3.0/7.0 \cdot 10^{18}$ cm^{-3} as defined for 65 nm/45 nm technology node.

In the above subsection the RTA process parameters that affect ultra-shallow junctions formed by SPEG were presented for boron and BF_2–implants and explained within the framework of the SIMS dopant distribution profiles. Now their interpretation in the R_s vs. X_J figure is discussed. All the sheet resistance and junction depth data for the annealing of the boron and BF_2 samples at various temperatures are summarized in Fig. 5.

Fig. 5 shows that the results from SPEG processes are inside the boundaries set for 70 nm and 65 nm technologies, and they come close to the 45 nm technology node requirements in the case of an implant of $^{11}B^+$, 500 eV at a dose of $1.0 \cdot 10^{15}$ cm^{-2} in a ^{73}Ge-preamorphized layer (30 keV $1.0 \cdot 10^{15}$ cm^{-2}) and a tightly controlled RTP solid-phase epitaxial growth process.

CONCLUSIONS

In this contribution the important anneal parameters (thermal budget and gaseous ambient) for producing highly activated solid-phase epitaxial grown junctions are discussed. With germanium preamorphized samples implanted with 500 eV, $^{11}B^+$, $1.0 \cdot 10^{15}$ cm^{-2} the technology requirements for the 65 nm node can be satisfied using a lamp-based RTP system for the regrowth process. The position of the end-of-range damage for this process needs to be optimized so that the defect-induced leakage current is minimized. The optimal process for high activation during SPEG is around 650°C for 5 s to 60 s in an inert argon ambient. Post-SPEG thermal processing at temperatures higher than 700°C can dramatically increase the junction depth, degrade abruptness and lead to deactivation. For this reason it seems that a low temperature silicide process like for NiSi also with low silicon consumption is necessary.

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REFERENCES

1. International Technology Roadmap for Semiconductors 2001 Edition, Dec. 2002, Semiconductor Industry Association (SIA), San Jose, CA
2. W. Lerch, B. Bayha, D.F. Downey, E.A. Arevalo, *Electrochemical Society Proceedings* **2001-9**, (2001) 312-336
3. S. Paul, B. Bayha, W. Lerch, C. Merkl, D.F. Downey, E.A. Arevalo, *IIT2002 conference*, Taos, New Mexico. Presented and accepted for publication.
4. L. Csepregi, J. Gyulai, S.S. Lau, *Materials Chemistry and Physics* **46** (1996) 178-180
5. B. L. Crowder, *J. Electrochem. Soc.* **117** (6) (1970) 671-674
6. B. L. Crowder, *J. Electrochem. Soc.* **118** (6) (1971) 943-952
7. K. Tsui, K. Takeuchi, T. Mogami, IEDM Tech. Dig. (1999) 9-10

8. H. Shimada, I. Ohshima, S.-I. Nakao, M. Nakagawa, K. Kanemoto, M. Hirayama, S. Sugawa, T. Ohmi, IEDM Tech.Dig. (2001) 67-68
9. Y.C. Yeo, V. Subramanian, J. Kedzierski, P. Xuan, T.-J. King, J. Bokor, C. Hu, *International Semiconductor Device Research Symposium*, Charlottesville, VA (1999) 295-298
10. J. O. Borland, *Solid State Technology* **6** (2002)
11. W. Magee, J. R. Shallenberger, M. S. Denker, D. F. Downey, M. Meloni, S. D. Cloherty, S. B. Felch, and B. S. Lee, *Proceedings of the Ultra-shallow junction Workshop,* April 1997
12. G.L. Olson, *Mat. Res. Soc. Symp. Proc.* **35** (1985) 25-38
13. G.L. Olson, J.A. Roth, L.D. Hess, J. Narayan in "Layer structures and Interface Kinetics", ed. by S. Furukawa, Tokyo: *KTK Scientific* (1985) 73-98
14. E. Landi, S. Guimaraes, S. Solmi, *Appl. Phys.* **A4** (1987) 135-141
15. W. Lerch, M. Glück, N. A. Stolwijk, H. Walk, M. Schäfer, S. D. Marcus, D. F. Downey, J. W. Cho, J. Electrochem. Soc. **146** (7) (1999) 2670-2678
16. C. Bergaud, D. Mathiot, L. Laanab, A. Claverie, A. Martinez in "Ion Implanation Technology 1994", ed. by S. Coffa, G. Ferla, F. Priolo, E. Rimini, *Elsevier Science B.V.* (1994) 756-758
17. S. Paul, W. Lerch, D.F. Downey, A. E. Arevalo, to be presented at *7th International Workshop on: Fabrication Characterisation, and Modelling of Ultra-Shallow Doping Profiles in Semiconductors*, April 27th – May 1st 2003 Santa Cruz, CA