PROCESS INTEGRATION OF PHOTORESIST STRIPPING, BARRIER REMOVAL AND COPPER TREATMENT FOR ADVANCED BEOL APPLICATIONS

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As the dimensions of ultra-large scale integrated (ULSI) devices continue to scale down, the process performance requirements for each individual process step become more stringent. In addition, integration and optimization of multiple process steps in a single process module has become crucial for meeting advanced device performance and reduction of manufacturing cost. In the back-end-of-line (BEOL) processing, dual-damascene has become the standard process flow for advanced copper/low-k technology. Appropriate integration of several steps in this process flow can significantly improve process performance, increase productivity and reduce cost. In this paper, an integration scheme of combining photoresist stripping, copper barrier removal and copper treatment (3-in-1 integration) for damascene processes is discussed. The use of a high-density plasma reactor operating at low pressure with independent control of ion density and ion bombardment energy has shown advantages of high photoresist strip rate, good profile control, nor or minimal low-k damage and effective cleaning of copper surface. Key knobs and approaches have been found to achieve robust process performance for mass production.

INTRODUCTION

The requirements for high signal processing speed in ULSI devices at the 90nm node and beyond have fostered the adoption of copper/low-k technology for BEOL interconnects [1]. Several different plasma etching and cleaning steps are needed in the standard dual-damascene process flow used to create copper interconnects and contacts, including low-k via and trench etching, stop layer and barrier layer removal, organic film recessing, photoresist stripping, and copper surface treatment [2]. In order to achieve designated device performance, optimal integration of these process steps is critical, especially when the k value of the dielectric film is further reduced with a resultant increase in susceptibility to low-k film damage from exposure to plasma processes. On the other hand, successful process integration can also effectively enhance productivity and lower costs in mass production. Several different approaches using different process tools have been used to integrate two or more of these process steps. In a non-integrated

approach, low-k film etching, barrier removal and photoresist stripping are done in separate tools. This approach requires frequent wafer transfer between different tools and thus lowers overall fab productivity. It also increases the chance of defects due to long copper exposure to the atmosphere. In another approach, all etch and strip steps are performed in the same tool, usually a dielectric etcher. The major challenges of this approach include minimizing the interference between steps that use different chemistries and generate different etch by-products, maintaining a highly stable process environment and achieving high throughput with low production cost.

In this paper, we present an alternative integration scheme for both single- and dual-damascene process flows. The key point of this novel approach is to separate via and trench etching from barrier removal, photoresist stripping and copper treatment. The process regimes required for these two sets of process steps diff in terms of process conditions, gas chemistries and by-product generations. By using a high-density plasma reactor operating at low pressure with independent control of ion density and ion-bombardment energy, a "3-in-1" process integration involving photoresist stripping, barrier removal and copper treatment has demonstrated high strip rate, good profile control, minimal low-k damage and effective treatment of the exposed copper surface. High process stability has also been verified through extensive tests to ensure robust process performance for mass production.

EXPERIMENTAL

This work was performed in an Aspen III Highlands strip system from Mattson Technology. Each process chamber has two separate plasma compartments so two wafers can be processed at the same time. Each of the compartments has its own RF system for plasma generation and control, but they share the same gas line and pump. As shown in Fig.1 for a compartment, the high-density plasma is generated by a RF power (source power) of 13.56MHz applied to an inductive coil on a dielectric dome, which is set on a Faraday shield mounted on the top plate of the chamber. The Faraday shield is grounded to filter out the capacitive coupling. The wafer is held on a temperature controlled cathode. A separate RF power (bias power) of 13.56MHz is applied to the cathode to control ion bombardment energy to the wafer. The chamber is evacuated by a turbo-molecular pump backed by a dry mechanical pump. Process gases are introduced through the nozzle at the top of the dome with controlled flow rates. Chamber pressure is maintained at a designated value with a throttle valve. Process endpoint control is done by an optical emission spectroscopic system.

The patterned wafers used in this work have either a single-damascene or dual-damascene structure on various low k dielectric materials, with vias and trenches already etched on separate dielectric etchers. At the bottom of vias, there is a copper barrier layer of $\leq$ 500Å thick which is either SiN or SiC film. Process results were inspected using scanning electron microscope.

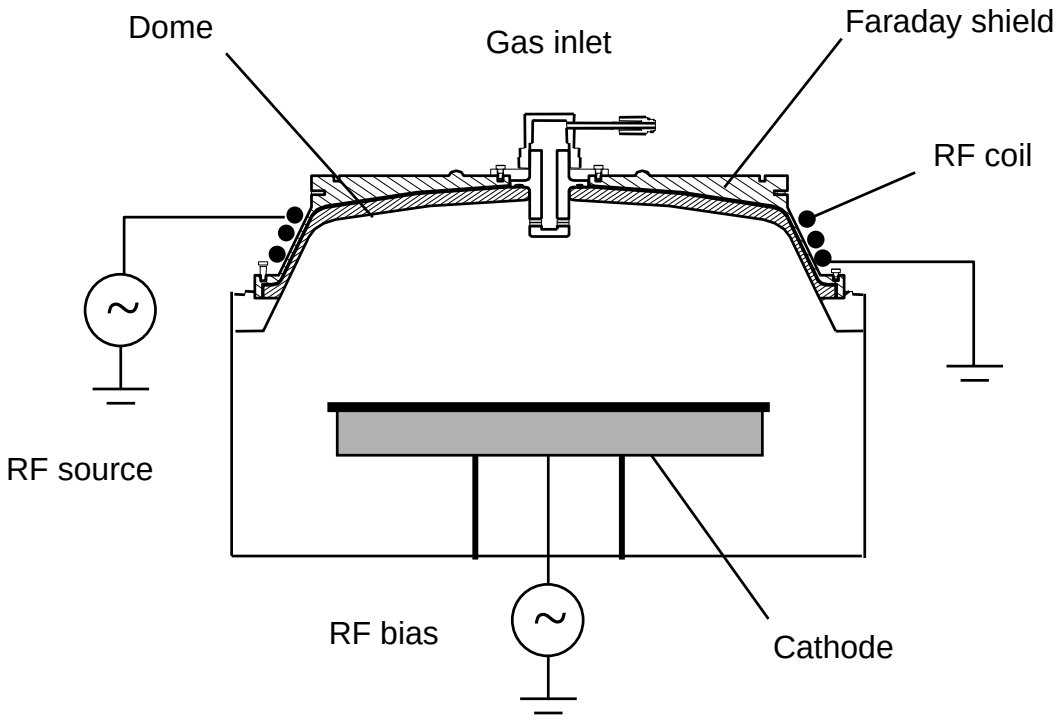

Fig.1 Schematic diagram of Highlands plasma reactor.

RESULTS AND DISCUSSION

The process flow of the 3-in-1 integration scheme is shown in Fig.2, which starts after the via and trench have been etched in a separate dielectric etcher. In the first step, the photoresist is stripped. The copper barrier layer is then removed, followed by copper treatment. An alternative process flow is to remove the barrier first, then strip the photoresist, finished by copper treatment [3]. Since the first approach prevents the exposure of copper to the resist stripping plasma, which is oxygen-based for most current applications, excessive oxidation of copper surface can be avoided [4]. Thus, it is the most commonly used one and will be discussed in detail in this paper.

For photoresist stripping on most low-k dielectrics ($k \geq 2.7$), O_2 plasma can be used without causing significant low-k damage. In high-density plasma reactors, such as the one used in this work, the resist strip rate increases monotonically with source power and bias power. However, it shows a maximum when pressure changes, as illustrated in Fig.3 with a fixed power level of 1200W for source and 100W for bias. Usually, a low pressure regime is chosen to obtain higher strip rate and better uniformity. Actually, the photoresist strip step also serves as a post–etch cleaning step for via and trench etching

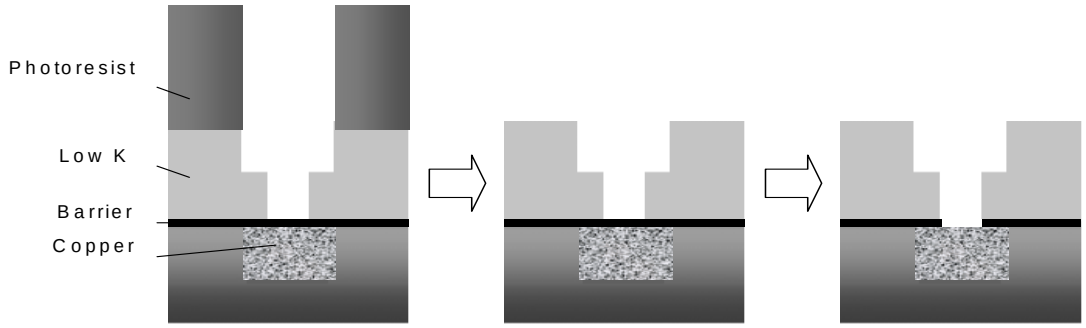

Fig.2 Process flow of 3-in-1 process integration.

that usually generates a lot of polymer residues on the sidewall and bottom surfaces. Since these residues typically contain both organic and inorganic components, their removal is more difficult than resist stripping itself. It has been found that the effectiveness of residue removal depends significantly on process conditions including pressure, source power and bias power.

For photoresist stripping on ultra-low-k dielectrics ($k \leq 2.4$) having high content of carbon, O_2 chemistry tends to cause serious low-k damage by causing significant carbon depletion and forming Si-O bonds. To preserve the k value, reducing chemistry is used instead [5]. Photoresist stripping with reducing chemistry is also run at a low pressure, not only to achieve higher strip rate but also to reduce low-k damage due to higher ion bombardment anisotropy. Fig.4 compares the RC constants of a test device obtained after the resist is stripped on porous methylsilsesquioxane-based dielectric material ($k = 2.2$) in O_2 and NH_3 plasmas at 10mTorr. The larger RC delay caused by O_2 plasma confirms the low-k damages. On the other hand, reducing chemistry produces very small change in k value and RC constant, although its strip rate is lower compared to O_2 chemistry under the same process conditions as shown in Fig.3.

After the photoresist is stripped, the copper barrier layer at the bottom of the via, which is either SiN or SiC, can be removed using fluorine-containing plasma. In order to prevent the formation of polymer residue on the copper, less polymerizing chemistry and process condition is selected. In many cases, the barrier can be etched with little residue by using pure CF_4 or a CF_4/Ar mixture, while good etch profile and critical dimension (CD) control can be achieved by optimizing the process conditions, including pressure, source power and bias power. In general, low pressure helps to reduce profile bowing and low-k damage as the isotropic chemical etching is reduced. Proper combination of source power and bias power is also vital to obtain vertical profile and small CD variation. Fig.5

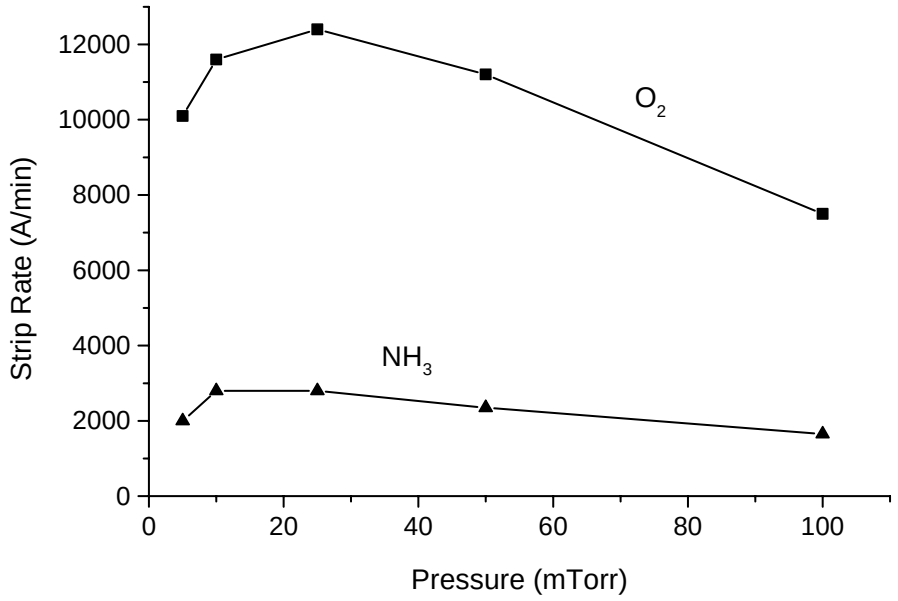

Fig.3 Dependence of photoresist strip rate on pressure.

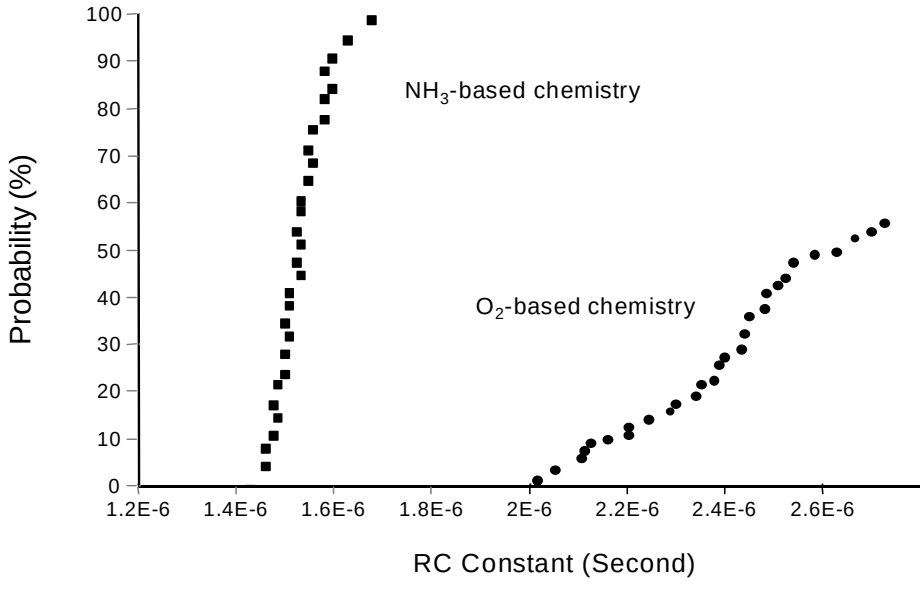

Fig.4 Effect of photoresist strip chemistry on RC constant.

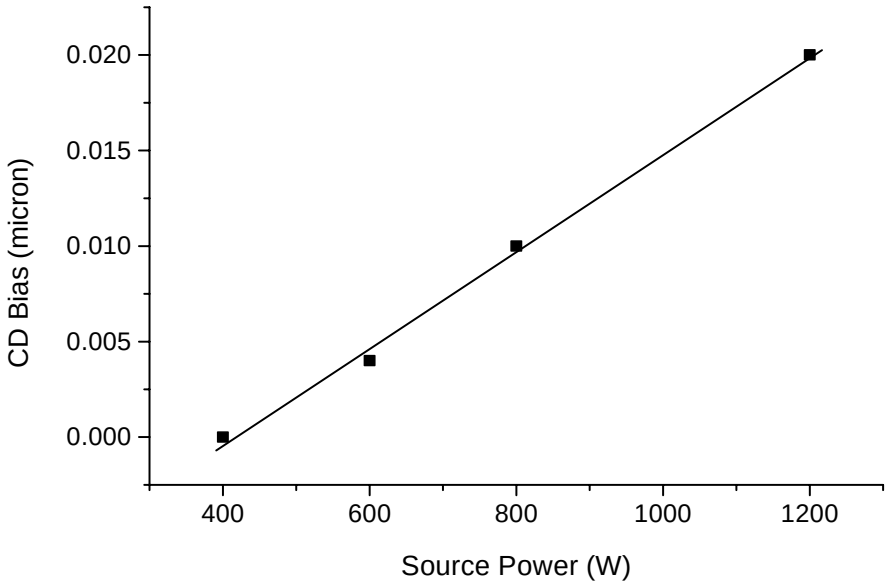

Fig.5 Source power dependence of CD bias after barrier removal.

shows the source power dependence of CD bias for the via after barrier removal in CF_4-based plasma. It is obvious that higher source power tends to cause larger CD loss. Higher bias power increases ion bombardment energy and anisotropy which generally reduces profile distortion and CD loss, as well as clean the residue at the via bottom. But high bias power might also cause copper sputtering during the overetch of barrier removal. Serious copper sputtering can cause contamination issues and affect device performance. In high-density plasma reactors like the one used in this work, the ion bombardment energy can be controlled over a large region from ~10eV to a few hundred eV, making it relatively easy to optimize different process performance simultaneously. A typical process result of copper barrier etching is shown in Fig.6.

The last step in the 3-in-1 process integration scheme is copper treatment. After the barrier removal, some polymer residues might be left on the copper, and the copper surface is also fluorinated. Since both of these can significantly affect the electrical performance of the devices, it is very important to have them cleaned before going to the subsequent process steps [6]. Copper cleaning can be done with wet cleaning methodology, but it is difficult to achieve high cleaning efficiency, especially after the wafers have been exposed to the moisture in the atmosphere for a long period of time. To overcome this problem, the most straightforward and simple approach is to have the copper surface treated right after the barrier removal without removing the wafers out of the chamber. Among several chemistries tested based on oxygen, nitrogen, hydrogen and

argon, it has been found that hydrogen is the most effective one. The surface reactions involved are basically the following two reducing processes:

$$\text{Organic polymer (C, H, F, …)} + H \rightarrow CH_x + HF + \ldots$$

$$CuF_x + H \rightarrow Cu + HF$$

In the first reaction, hydrogen cleans the organic residues by forming volatile hydrocarbon and hydrogen fluoride by-products. In the second reaction, copper fluoride is reduced, making the copper surface more stable in the atmosphere. The efficiency of copper treatment depends not only on the chemistry but also on the process conditions. Fig.7 compares the results of an effective copper treatment and an ineffective one where residue is found. So far, highly effective copper treatment has been obtained in the high-density plasma reactor used for this work at low pressure regimes with appropriate ion flux and bombardment energy. Effective in-situ plasma copper cleaning can reduce the load or even eliminate the need of post-etch wet treatment.

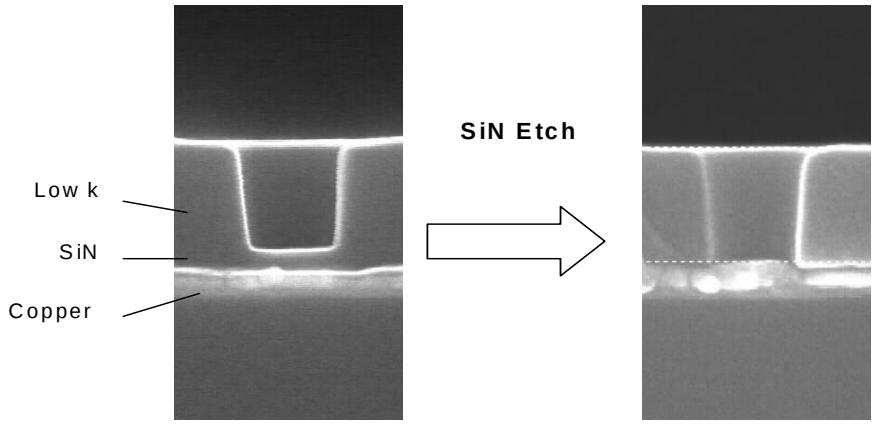

Fig.6 Process performance of copper barrier removal.

The 3-in-1 process integration scheme discussed above has shown advantages not only in process performance but also in process productivity. Since via and trench etching are not conducted in the same chamber, and there is almost no polymer deposition to the chamber wall during copper barrier removal, the whole process is basically run at a clean mode. Such a clean process has at least two major advantages for productivity. First, there is no deposition-related particle and defect issue. As a result, no frequent chamber cleaning during production is needed. In contrast, when via and trench etching are also done in the same chamber, chamber cleaning may be required as frequent as every wafer pass. This significantly lowers the throughput in device production. Second, the

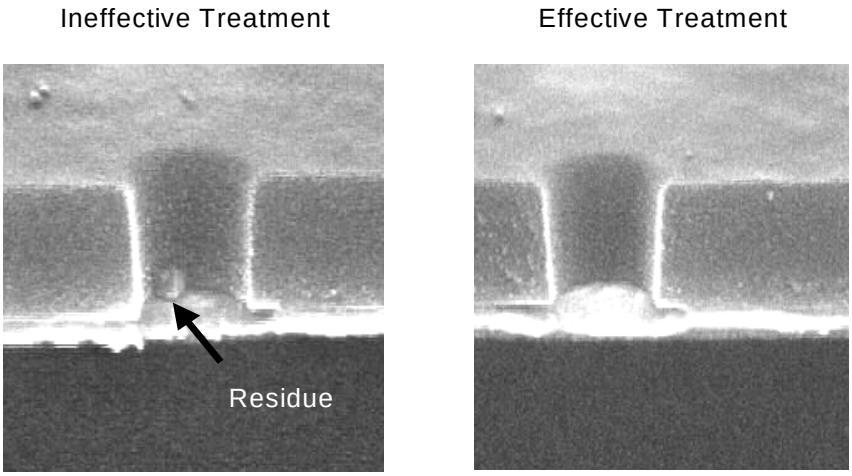

Fig.7 Comparison of effective and ineffective copper treatment.

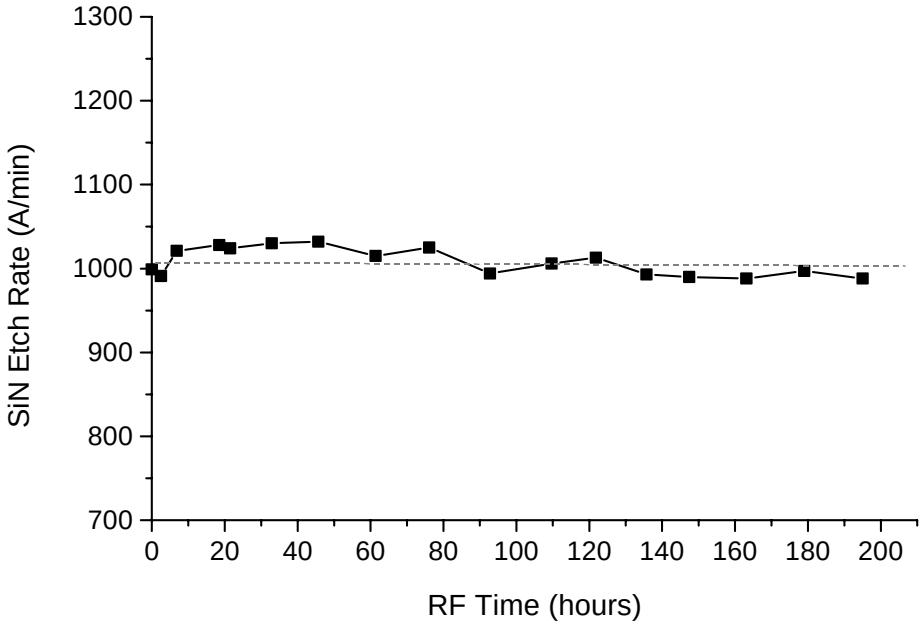

Fig.8 Process stability of 3-in-1 process.

chamber wall condition can be kept almost unchanged. It is well known that changes in chamber wall conditions can cause variation in plasma properties and, thus, process performance [7, 8]. The organic polymer deposition on the chamber wall will make the resist strip rate to change, the dielectric film etch rate and selectivity will also be affected. By using a clean process integration, the process performance can be kept stable. As an example, Fig.8 shows the very stable SiN barrier removal rate over 200 RF hour continuous running of 3-in-1 process.

CONCLUSION

The 3-in-1 process integration of photoresist stripping, barrier removal and copper treatment is an advantageous alternative approach for copper/low-k damascene applications. By using a high-density plasma reactor operating at low pressure with separate control on ion density and ion bombardment energy for this approach, several process advantages can be obtained. In the photoresist stripping step, the resist strip rate is high, while preserving the low-k film integrity. In the barrier removal step, profile control is good and process window is quite wide. No polymer deposition makes it possible to keep a clean chamber status for the whole process, stabilizing the chamber surface condition and preventing particle and defect generation. In the copper treatment step, no copper exposure to oxygen and moisture before treatment, effective copper treatment is done by hydrogen plasma in a short process time. The high efficiency of each step reduces the overall process time, enabling high throughput and low production cost.

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