UV-Enhanced Oxynitridation of Silicon Substrates

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Abstract

The fundamental limit to the scaling of thin SiO_2 for ultra large scale integrated (ULSI) circuits is the large leakage current due to direct tunneling. Oxynitride films have been investigated as gate dielectrics due to their enhanced reliability relative to SiO_2 with comparable equivalent oxide thickness (EOT). In this paper we show the formation of an oxynitride layer on silicon using a novel UV-enhancement technique. The substrate is exposed to UV radiation in an ambient containing O_2 and N_2. UV radiation is emitted from an external Xenon lamp with a broad wavelength (200-1100 nm) output. The photon energies from such Xenon lamp are 6.2 - 1.1 eV. We have used this UV-enhanced oxy-nitridation as the first step in a 4-step gate stack process, which is described below. The oxynitride thickness is about 6 Å based on an analysis of ellipsometric and electrical data of the final gate stack.

Prior to the oxynitride formation the silicon substrate surface was cleaned with UV-excited ozone to remove organic residues. A HF-methanol vapor treatment was then applied to remove any grown oxide. Finally, UV-excited chlorine was used to remove metallic contaminants. After this pre-cleaning step, the silicon substrate was exposed to UV radiation, at a power of 100-200 W, in an atmosphere consisting of 2-12% O_2 in N_2, for 30-90 s at 100-150°C and 80-120 Torr, resulting in the formation of a thin oxynitride film. A film of silicon nitride was then deposited over the oxynitride layer using a chemical vapor deposition (CVD) process at 750°C. The substrate was then annealed in an NH_3 ambient at 900°C and 450 Torr. Finally, the substrate was annealed in a N_2O atmosphere at 800°C and 450 Torr. The composite oxynitride gate stack dielectrics layers formed on the silicon substrate using this method have substantially improved performance, with EOT values as low as 14.2 Å. The associated leakage current densities are in the order of $1x10^{-1}$ Ampere/cm^2. For the 100nm node, the MPU gate dielectric EOT shall be 13 Å thick with leakage current density less than 1.0 Ampere/cm^2.

Introduction

As the channel length of the MOSFET is reduced the gate dielectric thickness must be reduced in order to maintain acceptable short-channel effects and to maximize drain current. The fundamental limit to the scaling of thin SiO_2 is the large leakage current due to direct tunneling [1,2]. Oxide/nitride composite layer has been employed to improve the performance and reliability [3]. However, when the equivalent oxide thickness (EOT) of the SiO_2/Si_3N_4 structure is reduced below 20 Å as is required in the ITRS Roadmap for advanced technology nodes, alternative high-permittivity (K) dielectrics such as Ta_2O_5 or ZrO_2 must be considered [4,5]. Electrical characteristics of an 0.1 μm transistor with Ta_2O_5 dielectrics has been reported [6]. MOSFET with ZrO_2 of 15 Å in EOT has also been reported previously [7].

Most high-K materials can be grouped into two general categories. (a) Materials that are stable with Si, such as ZrO_2 (K=25), HfO_2 (K=30), Al_2O_3 (K=11.6), Y_2O_3 (K=14), La_2O_3 (K=20.8), and Zr and Hf silicates (K=11). (b) Materials that are not thermally stable with Si, such as TiO_2 (K=40-80), Ta_2O_5 (K=26), $SrTiO_3$ (K=150). For the latter category, a thin barrier layer is required to prevent reaction and inter-diffusion at the interface. Key issues critical to the development of high-K gate stack are: small EOT, low leakage current, good interface layer between high-K dielectrics and Si, thermal stability and gate electrode. We shall address these issues with respect to the thermal anneal of high-K dielectrics and the formation of interfacial layer.

High-K dielectrics may be formed by various novel techniques [7-10] such as physical vapor deposition, chemical vapor deposition, and atomic layer deposition. Thermal anneal has been found to reduce electrical leakage across the film, presumably by removing vacancies or other defects in the metal oxides. A problem in high-K gate stack involves unintentional low-K material formed at the interface during growth or post-deposition processing. Thermal stability of the high-K dielectrics is also an important property defining its use in conventional CMOS process flow in which high thermal budget cycles exist. Many studies have demonstrated the important role of post-deposition anneal by rapid thermal processing (RTP) techniques in determining the final properties of high-K dielectrics [11-14].

For most high-K thin gate dielectrics, the interface to Si is the dominant factor in determining the overall electrical properties. Even in the ideal case of completely eliminating interfacial reaction, the structure still contains several dielectrics in series, where the lowest-K layer will dominate the overall capacitance and set a limit on the minimum achievable EOT value. Numerous studies have been reported on the ultra-thin dielectric formation techniques, with increasing attention paid to low thermal budget RTP processes. RTP in appropriate ambient has demonstrated merits and potential in achieving good interface between high-K dielectrics and silicon [12-17].

Oxynitride films have been investigated as gate dielectrics due to their enhanced reliability, including higher breakdown fields, longer time-to-breakdown (T_{BD}), improved gate leakage, and less hot-carrier degradation relative to conventional oxides with comparable effective dielectric film thickness [19-23]. Incorporating nitrogen (N) into the gate dielectric has also been examined as a diffusion barrier

against boron in dual-gate CMOS technologies [24-26]. Oxynitride dielectrics have been grown by a variety of methods. Ammonia (NH_3), nitrous oxide (N_2O), and nitric oxide (NO) have all been used as nitriding agents [27-37]. Comparisons between N_2O and NO grown films have been extensively reviewed [26, 34]. It has been speculated that for both N_2O and NO ambients, NO is the reacting species [34, 38]. However, NO ambients are reported to produce films with higher peak maximum N concentrations, a different bonding structure, and narrower N distributions than N_2O grown films [26, 28, 29]. Re-oxidized oxynitride films (ReOx) grown by either method have shown superior electrical properties [20, 23, 39]. Long re-oxidation times appear to increase the dielectric film thickness and change the interface to a SiO_2/Si interface, and to decrease the N content of the film [29, 40, 41].

Furnace, RTP, ultra-high vacuum and remote plasma systems have all been used to produce oxynitride films [30,36,37,39,41,42]. N_2O decomposes to form NO and atomic oxygen O, the former reacts at the Si interface. In a typical furnace process this NO may recombine with O before reaching the wafer surface, limiting the amount of NO available for the reaction. With RTP, the N_2O decomposes at the wafer surface, thus increasing the amount of available NO. Narrower N distribution and higher maximum N concentration in the depth profiles have been observed for rapid thermal nitridation (RTN) when compared to similar furnace processes [43,44].

The single layer oxynitride dielectrics has been modified significantly for applications in the 180 nm technology node by a scheme of multiple layer composite dielectrics [45-47]. Most notable examples are those proposed by Kwong et al., as shown in Figure 1 [45]. The multi-layer composite dielectric is usually formed after a dry pre-clean process, that typically consists of three steps [48,49], namely,

UV-Ozone (100 Torr) + HF-methanol vapor (100 Torr) + UV-Cl_2 (10 Torr).

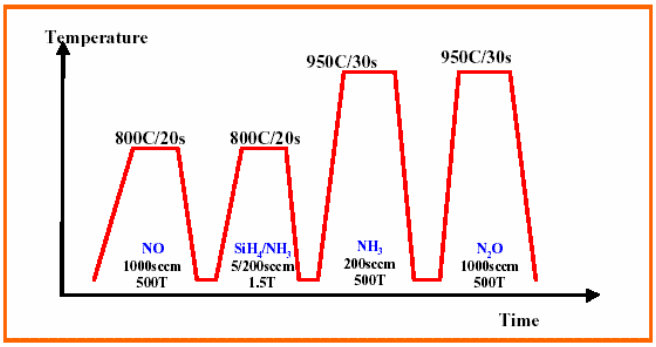

Figure 1. A typical multi-layer gate stack process

Kwong's composite dielectrics process generally comprises the following four steps:

NO (RTP, 20 s, 800°C, 100 - 500 Torr) – to thermally grow an oxynitride film;

+ NH_3/SiH_4 (CVD, 20 s, 800°C, 1.5 Torr) – to deposit a CVD SiN_x film;

+ NH_3 (RTP, 30 s, 950°C, 500 Torr) – to thermally densify the CVD SiN_x film;

+ N_2O (RTP, 30 s, 900°C, 500 Torr) – to re-oxidize the composite dielectrics.

The best EOT achieved and reported was 18.5 Å using this 4-step process [45].

In the 4-step gate stack process the first step is the most critical. The aim of this step is to grow an oxynitride layer of very low EOT, with appropriate nitrogen content; that allows proper nucleation of silicon nitride on the oxynitride layer. The surface roughness of a CVD silicon nitride film deposited on a silicon dioxide layer has been found undesirably high (*i.e.*, root mean square (RMS) roughness of about 10 Å and even up to 20 Å) when the physical thickness of the nitride layer is about 25 Å and below. Published research papers [50, 51, 52] have indicated that the coalescence of nitride nucleation islands does not take place until the physical thickness of the silicon nitride film exceeds ~20 Å. As the growth of silicon nitride films on oxide layers appears to be dependent upon having sufficient nucleation sites, thinner nitride films have had unacceptable surface roughness leading to unacceptable gate dielectric characteristics. Some studies have shown that remote plasma oxidation may improve the ultra-thin oxide interface [53]. Unfortunately, remote plasma oxidation requires special processing equipment and is complicated to use. Alternative approaches to create more nucleation sites and reduce surface roughness of the thin silicon nitride films are therefore being sought.

In this paper we show the formation of an oxynitride layer on silicon using a novel UV-enhancement technique. We have used this UV-enhanced oxynitridation as the first step in a 4-step gate stack process. The composite oxynitride gate stack dielectrics layers formed on the silicon substrate using this method have substantially improved performance

Formation and Characteristics of Multi-layer Dielectric Structure

An RTCVD 2-chamber system clustered with a dry clean module was used in this work. The chamber had a base pressure of $<5x10^{-8}$ Torr. Prior to the oxynitride formation the silicon substrate surface was cleaned with UV-excited ozone to remove organic residues. A HF-methanol vapor treatment was then applied to remove any grown oxide. Finally, UV-excited chlorine was used to remove metallic contaminants. After this pre-cleaning step, the silicon substrate was exposed to UV radiation in an ambient containing O_2 and N_2. UV radiation is emitted from an external Xenon lamp with a broad wavelength (200-1100 nm) output. The photon energies from such Xenon lamp are 6.2 - 1.1 eV.

Experimental matrix of the UV-enhanced oxynitridation was carried out at a power of 100-200 W, in an atmosphere consisting of 2-12% O_2 in N_2, for 30-90 s at 100-150°C and 80-120 Torr. This resulted in the formation of a thin oxynitride film. A film of silicon nitride was then deposited over the oxynitride layer using a chemical vapor deposition (CVD) process at 750°C. The substrate was then annealed in an NH_3 ambient at 900°C and 450 Torr. Finally, the substrate was annealed in a N_2O atmosphere at 800°C and 450 Torr.

The effect of surface cleaning on oxynitride thickness is very strong in NO oxynitridation. The in-situ pre-cleaning using only HF vapor results in much thicker oxide than that using all dry clean steps. Atomic force microscopy has been used to study the effect of UV-Cl_2 pretreatment on surface roughness of the CVD SiN_x deposited on oxynitrides grown in NO ambient [54]. UV-excited Cl_2 has been found to increase the density of nucleation sites on silicon substrate for CVD silicon nitride deposition. This novel process has been demonstrated to dramatically reduce the RMS roughness for a CVD silicon nitride film with thickness of 22.5 Å. Similarly the effect of UV-excited O_2 and N_2 has been found to be significant as shown in Figure 2.

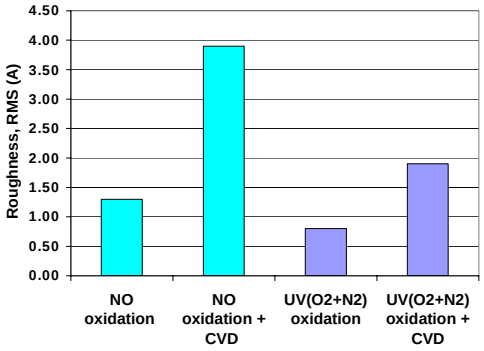

Figure 2. Effect of UV- N_2 + O_2 on Surface Roughness.

The oxynitride thickness is about 6 Å based on an analysis of ellipsometric and electrical data of the final gate stack. The composite oxynitride gate stack dielectrics layers formed on the silicon substrate using this method have substantially improved performance, with EOT values as low as 14.2 Å. A capacitance-voltage plot for the composite oxynitride gate stack is shown in Figure 3.

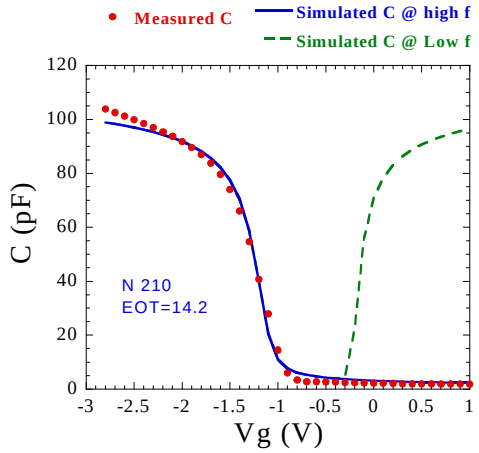

Figure 3. A capacitance-voltage plot for the composite oxynitride gate stack.

Figure 4 plots the leakage current densities versus EOT for various dielectrics. The leakage current densities for the composite gate stack dielectrics consisting of the UV-enhanced oxynitrides are in the order of $1x10^{-1}$ Ampere/cm^2. These data appear to extend the capability of the more conventional DLK 4-step process [45]. For the 100 nm node the gate dielectric EOT shall be 13 Å thick with leakage current density less than 1.0 Ampere/cm^2.

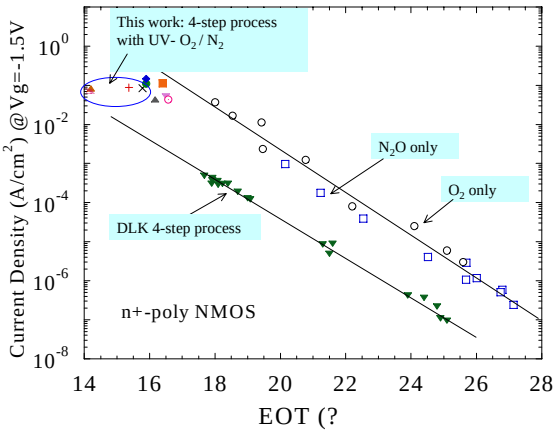

Figure 4. Plots of Leakage Current Density vs. EOT for various dielectrics including composite oxynitride gate stacks formed with UV- N_2 + O_2 (this work) as the first step in the more conventional DLK 4-step process [ref. 45].

Potential Applications in Hi-K /SiO_xN_y /Si Structure with Poly-Si/TiN or TaN Metal Gate

When the EOT of the composite gate stack is reduced below 20 Å, alternative high-permittivity (K) dielectrics such as Ta_2O_5 or ZrO_2 must be considered. Earlier studies of Ta_2O_5 (K=26) [12-14, 49, 55, 56] has shown that this material is not thermally stable with Si. A thin barrier layer is therefore required to prevent reaction and inter-diffusion at the interface. Substrate preparation typically requires RTN in ammonia ambient prior to Ta_2O_5 deposition. The RTN-formed SiO_xN_y layer also serves to prevent the Si surface from being oxidized during Ta_2O_5 CVD deposition as well as slow down interfacial oxidation during post-deposition anneal of Ta_2O_5 in oxygen-containing ambient. The refractive index of the RTN-grown SiO_xN_y film is ~2, and is independent of the RTN temperature. The film thickness changes from ~12Å @ 700^{o}C to ~25 Å @1100^{o}C. It is thus confirmed that SiO_xN_y, very close to Si_3N_4, was formed at temperatures as low as 700^{o}C [56].

The authors, in collaboration with Park et al.[12-14], have reported that SiO_xN_y/Ta_2O_5 stacked gate dielectric, with Poly/TiN gate, exhibits 3-5 orders smaller leakage current than SiO_2 at 18 Å while the transistor characteristics such as mobility, I_d-V_g, and I_d-V_d, are similar to those of SiO_2 transistor. N-channel MOSFET with EOT down to 18 Å has been demonstrated. Further reduction of interfacial nitride thickness may be possible with the use of UV-enhanced nitridation.

For the 90nm technology node and beyond ZrO_2 and HfO_2 have been favored by various groups of researchers. Kwong's

group [57] has reported MOS characteristics of ultra thin ZrO_2 dielectrics which was deposited on NH_3-treated silicon substrate at 475°C. The boron penetration characteristics were compared using PMOS transistors with and without NH_3-annealed interface layer. RTA drive-in performed at 800 - 1000°C showed that the boron penetration could be suppressed by a thin nitride (<5 Å) interface.

The authors, in collaboration with Kwong's group, have fabricated MOS capacitors with ZrO_2 /SiO_xN_y gate stack on p-type (100) epitaxial Si wafer for RTP anneal study [58]. The thicknesses of interface SiO_xN_y and ZrO_2 film are about 5 and 40Å, respectively. The electrode is TaN of 1800-2000 Å for the capacitors. Low leakage current of 50mAmpere/cm^2 at Vg = -1V is observed. The EOT for ZrO_2 film annealed in N_2 at 800°C for 60 s is 14 Å. Forming gas or wet-H_2 appears to retard interfacial oxidation. Leakage current values were measured at Vg = -1 V. ZrO_2 films with EOT of ~18Å exhibits leakage current density of approximately 10^{-5} Ampere/cm^2, nearly five order-of-magnitude lower than that for SiO_2 films with the same thickness. Physical thickness of ZrO_2/SiO_xN_y composite film has been determined by spectroscopic ellipsometry. Using the EOT value determined by C-V measurements the dielectric constant for ZrO2 has been estimated as K = 18.

The above experiment reveals the importance of RTP anneal ambient to the quality of ZrO_2/Si interface. Further work is needed to demonstrate the effect of interfacial morphology on the nucleation of ZrO_2 in a CVD process. A comparative study of thermal nitride and UV-enhanced oxynitride as interfacial barrier between ZrO_2 and Si substrate may be worthwhile.

Conclusions

In this paper the formation and characterization of some multi-layer gate stacks are reported. Emphasis has been made to correlate the interfacial barrier with the performance of the nitride and high-K dielectrics. The UV-enhanced oxynitride at the interface has demonstrated potential capability to improve leakage current density as the EOT continuously scales down in the future technology nodes.

Acknowledgments

The authors wish to acknowledge Prof. D.L. Kwong and Mr. C.H. Lee for their contribution to the ZrO_2 and SiO_xN_y work reported in this paper.

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